MOHD YUSUF YASIN, Ph.D.
Assistant Professor, Department of ECE, Faculty of Engineering,
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PROFILE

QUALIFICATION	• Ph.D.(Power Minimization in Electronic Circuit Building Blocks in Deep Sub-micron, Integral University, Lucknow, 2014) • M.Sc.Engg (Electronic Circuits and System Design, AMU, Aligarh, 1997, Ist Div.) • B.Sc.Engg (Electrical Engg, AMU, Aligarh, 1988, Ist Div.
RESEARCH AREAS	• Low Power VLSI Design, Circuits and Systems, Devices, Digital/Analog Signal processing.
TEACHING/ RESEARCH/ ESTABLISHMENT EXPERIENCE	32 years : 28 years (Integral University) + 3 years (AEC, Bhatkala, Karnatak University) + 1 year (Research Assistant, ECE, AMU Aligarh) (Asst. Prof.- 20 years; Lecturer - 11 years,; Research Asst - 01 year); Establishment experience of about 09 years of various institutional facilities and infrastructure at the Integral University, Design of syllabi of various B.Tech/M.Tech subjects both at the IIT Lucknow (now Integral University Lucknow) and, lab Development at AEC Bhatkala, Karnatak University. Specific details including Lab requisites, Lab experiments etc, are:

	(i) – Electrical Machine Lab. (ii) – Electronic Devices and Circuits (EDC) Lab. (iii) – Integrated Circuits Lab. (iv) – Analog Filter Design Lab. (v) – Design of Course structure and the Syllabi of M.Tech. program in Electronic Circuits and Systems. (vi) – Electronic Instrumentation and Control Lab-(AEC,Bhatkal). (vii) – Devices and Circuits Lab (Design of Experiments; AEC,Bhatkal). (viii) – Integrated Circuits Lab (Design of Experiments; AEC,Bhatkal).
PUBLICATIONS	46 : int jn/ Conferences.
RESEARCH GUIDED (Since Aug-2017)	a) Ph.D. :Awarded : 04; Submitted :01, Ongoing – 01. (Memristor modeling and analog adaptive system design, Fractiobnal order system design, solar panels - defects and performance, solar power battery systems, TFET Modeling) b) M.Tech : Awarded – 26+ c) B.Tech : Awarded – 19
WORKSHOP/ QIP/ FDP/ SHORT COURSES	13
ACHIEVEMENTS/ RECOGNITIONS AT THE NATIONAL/ INTERNATIONAL LEVEL	1. Best M.Tech Thesis of 2011 Award by IEEE-Industrial Applications Society (IEEE – IAS), to the Thesis on **Low Voltage Low Power Redesign of CCCII in 45nm CMOS Technology and it's Analog and Digital Applications**, submitted by Firdaus Majeed, May – 2011 was selected 3rd Best by the IEEE IAS Students Chapter in the Masters' Thesis Competition -2011, Florida, USA. 2. This work is in collaboration with the CHONGQING UNIVERSITY, Chongqing, China **New Tunable SISO Filter Designed in 40nm CMOS for Bilateral Inverse and Buffer Filtering Applications**, Umar Mohammad, Fang Tang, Shu Zhou and Mohd Yusuf Yasin, Jn. of Circuits, Systems and Computers, (online), World Scientific, Vol.30, Issue 13, April-2021, *SCOPUS, INSPEC*, https://doi.org/10.1142/S0218126621502406. 3. This work was supported by the Special Assistance Program, SAP, at the Islamic University of Science & Technology-IUST, Awantipora, Kashmir, India for the up

	gradation and improvement of the Institutional Technical education and research quality. **A novel square wave generator based on the translinear circuit scheme of second generation current controlled current conveyor-CCCII**, Umar Mohammad, Romana Yousuf, Imtiyaz Anwar Md., Mohd Yusuf Yasin, 1(6):587, May ,2019, Springer, SN Applied Sciences, DOI: 10.1007/s42452-019-0608-z. 4. Best Research Award, NESIN - 2020, research paper entitled **Oxidation : A Dominant Process for reduced Efficiency of Solar Photovoltaic Modules**, Tarana Afrin Chandel, M.Arifuddin Mallick, M. Y. Yasin Int. conf. on Advanced Light-weight Materials and Structures (ICALMS 2k20), Elsivier, Materials Today, Oct 2019
REVIEWER	International Journals: • Circuits and Systems, Int. Jn., Scientific Research Publishing, USA, 2016 (3) • Informacije MIDEDM - Journal of Microelectronics, Electronic Components and Materials, Slovenia, 2017
	International Conferences on: • IEEE-BHU, October - 2016 • Circuits and Systems – IMPACT-2011, AMU Aligarh, ; • 8th IEEE Colq. on Signal Processing – Malaysia 2012; • Computational Methods in Science and Tech. – Greece-2014;
TECNICAL MEMBERSHIPS	• ISTE (LM) • IETE (LM, M – 116452) • IEEE (MEMBER)

RESEARCH I TERESTS

- Circuits and Systems
- VLSI Design, LPLV, Analog,
- Solar Energy
- Non Engineering:

SUMMARY OF RESEARCH ACCOMPLISHMENT:

- IAS – IEEE Best Research, M.Tech. Level, of 2011, **Low Voltage Low Power Redesign of CCCII in 45nm CMOS Technology and it's Analog and Digital Applications**
- Best Research Award, NESIN – 2020, **Oxidation : A Dominant Process for reduced Efficiency of Solar Photovoltaic Modules**, DOI: 10.1016/j.matpr.2020.01.473

- Special Assistance Program, IUST, Kashmir, **A novel square wave generator based on the translinear circuit scheme of second generation current controlled current conveyor-CCCII**, May 2019, Springer, DOI: 10.1007/s42452-019-0608-z.
- Collaboration with the CHONGQING UNIVERSITY, China**, New Tunable SISO Filter Designed in 40nm CMOS for Bilateral Inverse and Buffer Filtering Applications**, April-2021,*INSPEC*, doi.org/10.1142/S0218126621502406.

PROFESSIONAL MEM ERSHIPS

- ISTE, LM
- IETE, LM
- IEEE MEMBER

COURSE TAUGHT: COURSES RELATED, BUT NOT LIMITTED, TO THE FOLLOWING

- VLSI Design
- Devices, Modelling and Circuits
- LP & LV Analog Circuits
- SP/DSP

STUDENTS SUPERVISION

A) Ph.D Thesis – 4 – AWARDED, 1 – SUBMITTED, 1 – ONGOING.

- **Design and Analysis of Tunnel Field Effect Transistor for Low Power applications** – Vedvarat, October 2024. AWARDED
- **Memristor: Model file development for SPICE/ MATLAB environment and its application in Advanced Electronic Circuits and System** – Noor Fatima Siddiqui, December 27, 2023. AWARDED
- **Performance Evaluation of Solar Photvoltaic Module using Photoluminescence Image Analysis** – Tarana Afreen Chandel, 1.8.2022, under IE(India) sponsored project ID:RDDR2017015 – AWARDED
- **Memristor in Adaptive VLSI System design** – Mohd Ahmer - December 2021– AWARDED

B) M.Tech. Thesis – 26 (2009 – till date)

C) B.Tech. Final year Projects – 19

PUBLISHED/GRANT PATENTS

Application No.: 202111035684, LOW COST MICRO CRACK MEASURING INSTRUMENT FOR DETECTION OF FAULTS ON SITE IN SOLAR PANELS. Published in August 2022. M. A. Mallick, M. Y. Yasin, MS. T. A. Chandel

PUBLISHED SCI/SCOPUS RESEARCH PAPERS

- **Technical and Economic Analysis of PV Integrated DC and AC in Front of the Meter System for Automated and Manual Dispatch Modes**, Aftab K. H., Asim M, Yasin M Y**,** IJISAE, Vol. 12, No.4, pp 860 – 869, https://ijisae.org, MCN: IU/ R&D/2024-MCN0002724, ISSN:2147-6799, Jun 2024.
- **Optimization of Dual Material Based Dielectric Modulated Heterojunction Double Gate Tunnel FETs with Noise Reduction Analysis for High Frequency Applications**, Vedvrat, M Y Yasin, Pandey D, SILICON Springer, vol-16, issue 9, pp 4061 – 4075, June 24. doi.org/10.1007/s12633-024-02987-w, MCN No: IU/R&D/2024- MCN0002486
- **Technical and Economic assessment of PV resource-based DC and AC connected behind the meter system for residential load**" Aftab H K, Yasin M Y, Asim M, IJISAE**,** vol 12, no 16s, pp 509 – 519, https://ijisae.org/index.php/IJISAE/article/view/4873/3563, MCN: IU/ R&D/2024-MCN0002461**,** ISSN:2147-6799, February 2024.
- **Improved Switching and Analog/RF Behaviour of SiGe Heterojunction Dielectric Modulated Dual Material Nano Silicon Tunnel FET for Low Power Applications,** Vedvrat, M Y Yasin, Vidyadhar Gupta, Digvijay Pandey, SILICON-Springer, issue 9, vol.16, Feb 24, doi.org/10.1007/s12633-023-02755-2, MCN No: IU/R&D/2023-MCN0002175.
- **A New Tunable SISO Filter Designed in 40nm CMOS for Bilateral Inverse and Buffer Filtering Applications**, Umar Mohammad, Fang Tang, Shu Zhou and Mohd Yusuf Yasin, Jn. of Circuits, Systems and Computers, (online), World Scientific, Vol.30, Issue 13, April-2021, *SCIE*/*ESCIE*,*SCOPUS, INSPEC*..., https://doi.org/10.1142/S0218126621502406.**
- **Memristor emulation and analog application using differential difference current conveyor of CC-II in CMOS technology**, M. Ahmer, N R Kidwai, M Y Yasin, ISSN:2214-7853(on line), Materials Today: Proceedings, Elsevier, Jun 2021, SCOPUS, INSPEC, doi.org/10.1016/j.matpr.2021.05.260.
- **Design Modeling and Simulation of 150 KW Solar Photovoltaic Systems: A Review**, Zoya Fatma, TA Chandel, M Y Yasin, Int. J. of Recent Tech. and Engg. (IJRTE), v.9 Issue 2, July 2020 ISSN: 2277-3878. *SCOPUS, NISCAIR, NSL***
- **Oxidation: A dominant source for reduced efficiency of silicon solar photovoltaic modules**, Tarana Afrin Chandel, M A. Mallick and M Y Yasin, Materials Today: Proceedings, vol. 27, no. part2, pp. 1092-1098, June 2020.
- **Performance of Rooftop Grid Connected Solar Photovoltaic System**, Tarana Afrin Chandel, M.Y Yasin and M A Mallick, International Journal of Recent Technology and Engineering, vol. 9, no. 1, pp. 1056-1062, May 2020.
- **Modeling and simulation of photovoltaic cell using single diode solar cell and double diode solar cell model**, Tarana Afrin Chandel, M Y Yasin, M A Mallick, Int. J. Innov. Tech. Explor. Eng.(IJITEE), v.8, issue 10, pp 557-565, August 2019, DOI: 10.35940/ijitee J8863.0881019, ISSN, DOI. SCOPUS,
- **Performance of Partially Shaded Solar Photovoltaic System**, T A Chandel, M A Mallick, M Y Yasin, IJRTE, vol.7, issue 6, ISSN:2277-3878, March 2019,S.No.247IF=1,SCOPUS, NISCAIR, NSL.
- **A novel square wave generator based on the translinear circuit scheme of second generation current controlled current conveyor-CCCII**, Umar Mohammad, Romana Yousuf, Imtiyaz Anwar Md., M Y Yasin, 1(6):587, May, 2019, Springer, SN Applied Sciences, DOI: 10.1007/s42452-019-0608-z **

- **Review on Solid State Thermoelectric Module and Its Use in Energy Recycling**, Irshad Ali, M Y Yasin, International Research Journal of Engineering and Technology IJRET, vol.03, issue 05, May 2016, pp 662 – 667.S. No.137.
- **Design of Low Cost Arm Control Robotic moving wheel chair for Elderly & Physically Disabled Persons**, U Mohammad, MY Yasin et. all, IJLSR, 2015; Vol. 1(4): PP144-148, ICI Indexed, ISSN: 2394-9864. DOI: 10.13040/IJPSR.0975-8232.IJLSR.1 (4).1-05**
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- **Low Voltage Low Power Redesign of CCCII in 45nm CMOS Technology and it's Analog and Digital Applications**, M.Tech. Thesis, Firdaus Majeed, M Y Yasin, May – 2011, Selected 3rd best by the IAS–IEEE, Vol.17, No.6, Nov.–Dec. 2011, pp. 74, ISSN 1077-2618, http://www.ieee.org/ias.
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- **Quadrature Oscillator – A New Simple Configuration Based On 45nm 2nd Generation CMOS Current Controlled Current Conveyor**, FirdausMajeed and M Y Yasin, Int. J. of Information and Computation Technology (IJICT), Vol. 2, No. 1, 2012, pp. 37-47, ISSN 0974-2239, http://www. ripublication.com.
- **High Frequency Oscillator Design Using a Single 45nm CMOS Current Controlled Current Conveyor (CCCII+) with Minimum Passive Components**, M Y Yasin, B Gopal, Int. Jn. of Circuits and Systems, 2011, 2, 53-59, doi:10.4236/cs.2011.22009 Published Online April 2011 (http://www.SciRP.org/journal/cs).

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- **Assessment of Dielectric Modulation on Switching Behavior and RF Performance of DM Tunnel FET for Digital Applications**., Vedvrat, Yasin, M. Y., & Tripathi, R, In International Conference on Power and Embedded Drive Control (ICPEDC - 2024). Springer Nature Singapore. (MCN No: IU/R&D/2024- MCN0002361)
- **Design and Assessment of Dielectric Modulated Dual Metal Tunnel FET for Low Power IOT Applications**, Vedvrat, Singh, R. K., Yasin, M. Y., & Rai, A. K., In 2024 2nd International Conference on Disruptive Technologies (ICDT), pp. 1027- 1031, IEEE Xplore, doi: 10.1109/ICDT61202.2024.10489394. (MCN No: IU/R&D/2024-MCN0002360)
- **DC Connected Solar Plus Storage Systems: An Overview**, Aftab K H, Yason M Y, Asim M, International Conference on Power, Instrumentation, Energy and Control (PIECON), pp- 1 – 6,

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- **A New Class of Bilateral SISO-(Single Input Single Output) Active Filters Targeted for Health-Care Applications** ,U. Mohammad, M. Y. Yasin and F. Tang, *2022 IEEE Bombay Section Signature Conference (IBSSC)*, Mumbai, India, 2022, pp. 1-5, doi: 10.1109/IBSSC56953.2022.10037285.
- **MEMRISTOR: APPLICATION AND MODELING**, Noor Fatima Siddique, Mohd Yusuf Yasin, Science, Technology and Development, Volume IX, Issue IV, APRIL, pp 179-197, ISSN: 0950-0707.
- **Oxidation : A Dominant Process for reduced Efficiency of Solar Photovoltaic Modules**, Tarana Afrin Chandel, M Y Yasin, M.ArifuddinMallick, Int. conf. on Advanced Light-weight Materials and Structures, ICALMS 2k20, Elsivier, Materials Today, Oct 2019**
- **Analog Signal Processing Applications of Current Mirror Amplifiers: A circuit design perspective**, Kamini, M Y Yasin, 28th July 2019, ICRTESM-19, Mahratta Chamber of Commerce, Industries and Agriculture, Tilak Road Pune, India, ISBN:978-93-87793-99-6,
- **Performance analysis of solar photovoltaic pannel using nanotachnology: a review**. TaranaAfreenChandel. M Y Yasin, M A Mallick,
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- **Model Parameter Extraction of Deep-submicron MOSFETs**, By Rubina Sheikh, Neha Tripathi, M Y Yasin, National Conference on Advance Research and Innovation, ARISE – 14, TeerthankerMahaveer University, Moradabad, May 17, 2014.
- **Low Power and High Speed Ternary OR Realization using a single transistor based CCCII-in 45nm CMOS Technology**, By Neha Tripathi, Rubina Sheikh, M Y Yasin, National Conference on Advance Research and Innovation, ARISE – 14, Teerthanker Mahaveer University, Moradabad, May 17, 2014.
- **An Analytical Delay Model for CMOS Inverter – Transmission Gate structure**, Mohammad Shoeb Roomi, Naushad Ali, M Y Yasin, IEEE sponsored International Conference on VLSI Design and Test, VDAT – 2014, 23-25 July 2014, PSG College of Technology, Coimbatore, India,.
- **CMOS Parameter extraction for Han-Held Design of Electronic Circuits in 45nm Technology**, Sheikh Rubina Banu, M Y Yasin, COTII-2014, Feb, AIMT Lucnow.
- **Low Voltage Low Power 45 nanometer CMOS Current Controlled Current Conveyor based Resistance free Phase Shift Oscillator Design**, M Y Yasin, B Gopal, National conference proceedings, Revolutionary Advancements in Communication and Electronics. RACE – 10, November 12,13- 2010, LIET, Alwar, Rajasthan
- **High Bandwidth, Low Power, High Performance Second Generation Dual Output Current Controlled Conveyor (DOCCCII)**, HasinAlam and M. Y. Yasin; International Conference on Modeling of Engineering and Technological Problems (ICMETP) January 2009 at B.M.A.S. Engineering College Agra.
- **High Frequency Oscillator Based On CCCII**, HasinAlam and M. Y. Yasin; Int. Conference on Modeling of Engineering and Technological Problems (ICMETP) January 2009 at B.M.A.S. Engineering College Agra.
- **Large Valued Capacitance Simulation**, Mohd Yusuf Yasin; presented at the Proceedings, National Seminar on Recent Trends in the Design of Electronic & other Engineering Systems, 29-30 Nov 1997.
- **Self Correction of the Phase Angle of the Non Ideal Standard Resistors, A Schematic Approach**, Mohd Yusuf Yasin, LITERATI-97, NIT, Krukshetra,

PUBLISHED PEER REVIEWED RESEARCH PAPERS

- **Non linear window function associated memristor application for design of spiking neuron circuit,** Noor Fatima, M Y Yasin, Neuro- Quantology, DEC 2022, Volume 20, Issue 19, Page 1201-1213, doi:10.48047/nq.2022.20.19.NQ99112.
- **An Improved Memristor Window Function with enhaced edge Non-Linearity application for Memristors,** Noor Fatima, M Y Yasin, Neuro-Quantology, July 2022, Volume 20, Issue 8, pp 2938-2949, doi:10.14704/nq.2022.20.8.NQ44325.
- **Memristor: Application and Modeling, Noor Fatima Siddique, M Y Yasin, vol IX, issue IV, April 2020,** pp 179-187, UGC, Web of Sc., DOI:20.18001.STD.2020.V9I4.20.33671
- **Noise Analysis of Class AB CMOS current conveyor: A review**, Kaynat Tabassum, M Y Yasin, JASC, vol. 6, issue 6, ISSN:1076-5131, June 2019. *UGC Approved,* Page No:2458-2461.DOI:16.10089.JASC.2019.V6I6.453459.1500101789.
- **SPICE Simulation of Memristor series and parallel**, M Ahmer, M Sajid, M Y Yasin, S-JPSET, v.9, issue 2, December 2017, ISSN: 2454-2767(online)/2229-7111(p), DOI:10.18090/ samriddhi.v9i02.10867, (MCN:- IU/R&D/2017-MCN000227). **UGC Approved** **
- **CNFET Based low voltage inverter design : the number of carbon nanotubes and the inverter performance**. Nudrat Sufyan, M Y Yasin, Int. Jn. For Innovations in Engineering, Science and Management (www.ijiesm.com), ISSN:2347 - 7911, vol-5, issue-6, June 2017.
- **Low Voltage Low Power and High Frequency VCO/ICO Design**, Mohammad Tayyab, M Y Yasin, Int. Jn. of Electrical and Electronics Communication Systems vol.1, issue 1, MAT Journals, pp : 11 – 21, July 2017.
- **CNFET: An alternative to conventional MOS for analog applications**, MohdMohsin, M Y Yasin, Irshad Ali, Umar Mohammad, IRJET, Vol.03, Issue 06, June 2016, pp-2859 - 2863, e-ISSN:2395-0056, p-ISSN: 2395-0072. S. No.533, UGC Approved.
- **Design and Soft Implementation of N-bit SRT Divider on FPGA through VHDL**, JyotikaKumari, M Y Yasin, International Journal for Innovations in Engineering, Science and Management, Vol. 3, Issue 4, April 2015 (www.ijiesm.com , ISSN 2347 - 7911)
- **Design and Comparative study of a fast N bit divider and it's VLSI Implementation**; Jyotika Kumari, M Y Yasin, Mohd Nadeem, International Journal for Innovations in Engineering, Science and Management, Vol. 2, Issue 11, Nov 2014, ISSN 2347 – 7911, www.ijiesm.com.
- **Design of 32 Bit CRC Generation using VHDL**, Mohd Zulqarnain Siddiqui, M Y Yasin, IJIESM, ISSN 2347 - 7911, vol. 3, isuue 2, Feb 2015, pp 06 – 12.
- **A novel bipolar XOR/XNOR realization using translinear type 2nd generation current controlled current conveyor designed in 45nm CMOS technology**, M.Y.Yasin, Acta*Electrotehnica, vol. 54, No.1, 2013, pp 3–6.*

MISCELLANEOUS RESEARCH PAPERS

- **Golden Ratio ϕ and the ϕ - Family, Characteristics and Features: An Iterative Approach**, M Y Yasin, Jn. of Applied Science and Engineering Research, Vol. 2; No. 2; June 2021 pp. 11-16, ISSN: 2691-6061 (Print) 2691-607X (Online), www.jaser-net.com, SCOPUS, Doi: 10.48150/jaser.v2no2.2021.a2.

- **Scientific Calculators and the Skill of Efficient Computation**, Mohd Yusuf Yasin, BIBECHANA 8 (2012) 31-36 : BMHSS, p. 31, ISSN:2091-0762 (online), http://nepjol.info/index.php/BIBECHANA
- **Complex roots of polynomials and their Computation with the help of Scientific Calculators**, Mohd Yusuf Yasin, BIBECHANA 8 (2013) BMHSS, p. 31 http://dx.doi.org/10.3126/bibechana.v9i0.7148
- **Simplified Approach To DFT Schemes For Non-Programmable Scientific Calculators**, Mohd Yusuf Yasin, BIBECHANA 12 (2015) 13-19, http://dx.doi.org/10.3126/bibechana.v12i0.11681.
- **Some Characteristics of Repeated Discrete Fourier Transformation**, Mohd Yusuf Yasin, Acta Electrotehnica, vol.57, no.5, 2016, pp 566-569

BOOK CHAPTERS

Chapter 14: **Performance Analysis of Rooftop Grid Connected Solar Photovoltaic System**, T. A. Chandel, M. Arifuddin Mallick, Mohd Yusuf Yasin

Advanced Aspects of Engineering Research Vol. 13, 12 May 2021, Page-156-181, https://doi.org/10.9734/bpi/aaer/v13/9364D,

ISBN: 978-93-91215-48-4,